SIW Power Divider and Its Performance Analysis Affected by Number of Incorporated CSRRs

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***Abstract*—This paper discusses the design of substrate integrated waveguide (SIW) power divider and its performance analysis affected by the number of incorporated complimentary split ring resonators (CSRRs). The proposed SIW power divider is designed on an FR4 epoxy dielectric substrate with the thickness of 1.6mm. The effect of increasing the amount of CSRRs incorporated into the SIW surface is analyzed for some parameters, namely frequency response, return loss, and insertion loss. Each CSRR is composed of a pair of concentric circle-shaped slot rings fitted with a gap in the opposite ends. The analysis results shows that the frequency response of SIW power divider decreases as the increase of number of CSRRs. Meanwhile the return loss and the insertion loss tend to be poorer for the higher number of CSRRs incorporation although the poorness of quality shows no particular pattern.**

***Index Terms*—complimentary split ring resonators (CSRRs), frequency response, performance analysis, substrate integrated waveguide (SIW)**

I. INTRODUCTION

During 2 last decades, the development of wireless communication system with data processing techniques and high data rate transmissions has grown up significantly. In its development, telecommunication devices are arranged with connecting channels or commonly called as transmission line [1]. Several configurations of transmission line have been investigated by many researchers so as to produce the desired characteristics for particular applications. A waveguide transmission line with dielectric substrates is one of the configurations frequently used in current wireless communication systems.

The waveguide transmission line involved in wireless communication systems is due to having low loss value, however it usually works at high frequency regions [2]– [3]. The waveguide transmission line is also considered more complicated in the manufacturing process as it has large size [4]– [5]. Meanwhile, the microstrip line can work at lower intermediate frequency, however it produces a greater loss value. Hence, the use of substrate integrated waveguide (SIW) method on microstrip line has been becoming a way out for the development in microwave applications [6]. The SIW method is preferred due to its capability in reducing production cost with high performance level. In practical, the SIW method is sometimes implemented by connecting coaxial connectors through microstrip transmission lines [7]–[8].

The basic material of SIW structure is commonly using a dielectric substrate with some thickness and certain relative permittivity. The SIW structure is configured by placing a sequence of via metals connecting the top metal surface and the groundplane [9]. The SIW structure which utilizes the concept of impedance by modeling a cylindrical sequence could be analyzed by combining the transversal resonance method. Here, the via metals serve as side walls of waveguide transmission line. Such structure can usually pass signals at high frequencies. In fact, the SIW method has a disadvantage as the structure introduces leakage losses into the surrounding circuit due to the spacing between via metals. To overcome this issue, some improvements have been proposed such as using half mode SIW [10], quarter mode SIW [11], and eight mode SIW [12]. Furthermore, in [13] a SIW method is designed using microstrip lone to produce an impedance characteristic of 50Ω. Whilst the modifications of SIW to be implemented in power divider has been performed using a rectangular patch with a box-shaped of CSRRs [14].

In this paper, the design of SIW power divider and its performance as the increase of amount of CSRRs incorporated into SIW surface is investigated. The performance of SIW power divider affected by the number of incorporated CSRRs is analyzed through its parameters, namely frequency response, return loss and insertion loss. The proposed SIW power divider is designed on an FR4 epoxy dielectric substrate with the thickness of 1.6mm. While the incorporated CSRRs are made of a pair of concentric circle-shaped slot rings fitted with a gap in the opposite ends. Some discussions of analysis results are presented and then followed by the conclusion.

II. DESIGN OF SIW POWER DIVIDER

To analyze the effect of number of incorporated CSRRs on the various parameters, the design is started by the SIW power divider with no CSRRs up to with 5 pieces of CSRRs. Figs. 1 and 2 illustrate the SIW power divider with no CSRRs and with 5 pieces of CSRRs, respectively. Each SIW power divider

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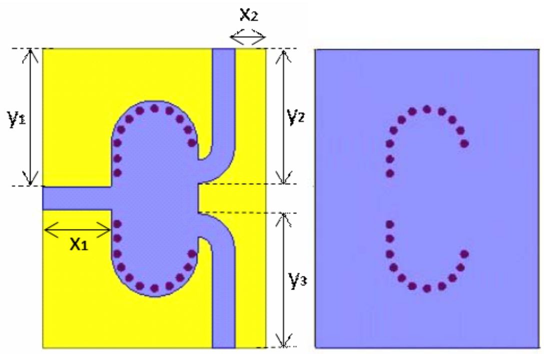

Fig. 1. Design of SIW power divider with no CSRRs; left is top side view; right is bottom side view.

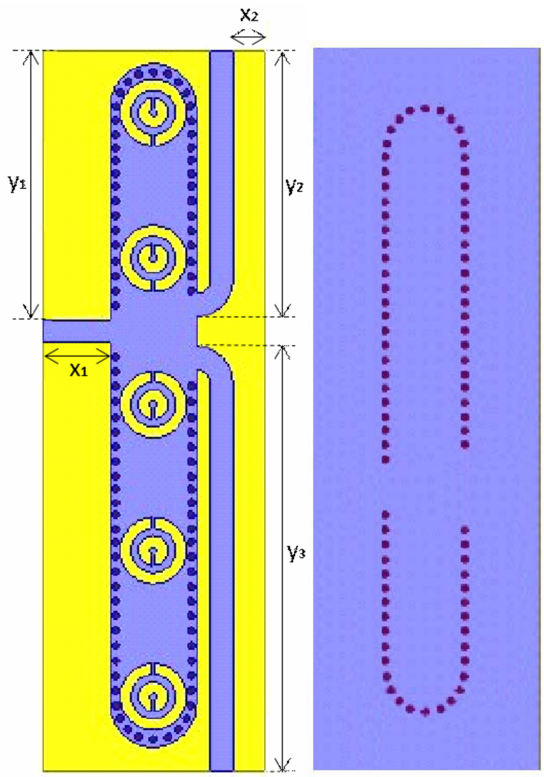

Fig. 2. Design of SIW power divider with 5 pieces of incorporated CSRRs; left is top side view; right is bottom side view.

is designed on a 1.6mm thick FR4 epoxy dielectric substrate with the width of SIW surface of 11.6mm. While the length of SIW surface as well as the number of via metals are adjusted upon the increase of number of CSRRs.

The incorporated CSRRs into SIW surface are made of a pair of concentric circle-shaped slot rings fitted with a gap in the opposite ends. Each CSRRs has the outer slot ring diameter of 9mm with the width of 1.5mm. Whilst the inner slot ring diameter is 4mm with the same width of 1.5mm. The gap between between outer and inner slot ring is set to be 0.5mm. The distance between CSRRs for 2–5 pieces of CSRRs is 19.7mm. The via metals with different amounts on each SIW surface depends on the number of incorporated CSRRs is used as the wall of waveguide referred to the SIW method. Here, each via metal has the diameter of 1mm and the separation with the adjacent ones of 1.4mm.

Furthermore, the proposed SIW power divider is designed to have 1 input port and 2 output ports. All the ports are made of microstrip lines with the width of 3.1mm yields to the impedance of 50Ω. The position of input port is adjusted by the number of incorporated CSRRs. The length of input port (x_1) as well as the distance of output ports from the edge of dielectric substrate (x_2) are kept to be fixed. While the length of input port 1 (y_1) and the length of output ports 2 and 3 (y_2 and y_3) are adjusted to the SIW surface length according to the number of incorporated CSRRs.

III. RESULT AND DISCUSSION

As shown in Fig. 3, the variation of number of incorporated CSRRs affects to the the value of return loss at the same frequency of 3.3GHz. The value of return loss for the SIW power divider with no CSRR is 0.387dB, while for the SIW power divider with 1, 2, 3, 4, and 5 pieces of CSRRs are 0.42dB, 1.035dB, 0.974dB, 0.958dB, and 0.88dB, respectively. Moreover, the value of insertion for the SIW power divider is plotted in Fig. 4. It shows that the SIW power divider should have the insertion loss value of 3dB for each port.

Then, the number of via metals is set to be 9 in each side of SIW surface for all amount of CSRRs. It shows in Fig. 5 that there is no bandpass response for the SIW power divider with no CSRRs. While for 1 piece of CSRR, the SIW power divider has a return loss of 5.113dB at the frequency of 3.2GHz. By increasing the number of CSRRs with 2–4 pieces, the values of return loss achieve 17.228dB at the frequency of 2.4GHz, 13.249dB at the frequency of 1.6GHz, 11.976dB at the frequency of 1.1GHz, for the SIW power divider with 2, 3, and 4 pieces of CSRRs, respectively. Whereas for the SIW power divider with 5 CSRRs, there is a value less than 10dB

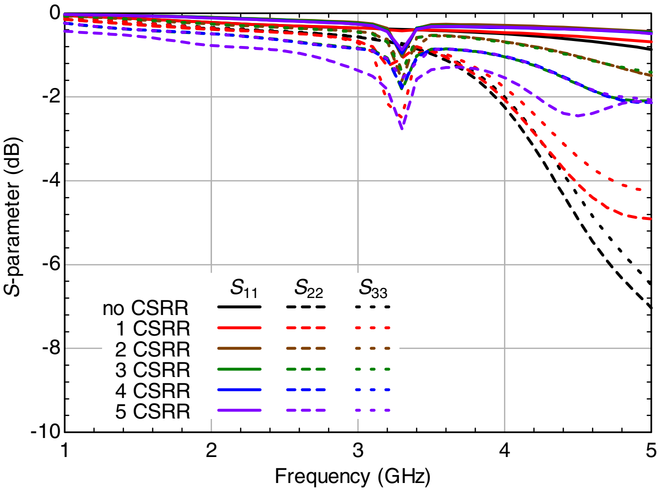

Fig. 3. Return loss of SIW power divider with and without CSRRs for adjusted number of via metals.

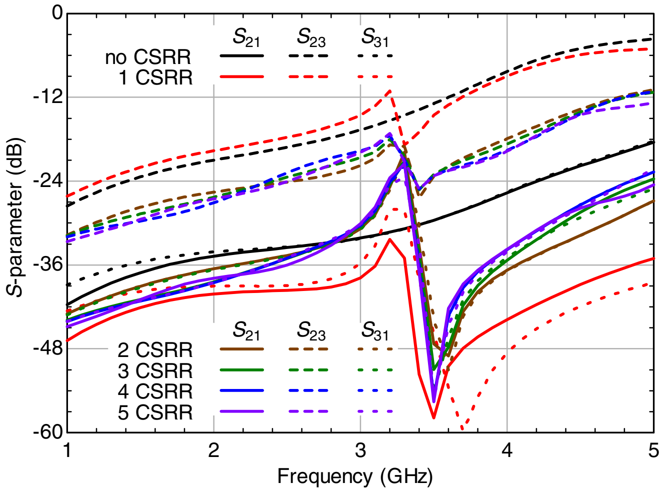

Fig. 4. Insertion loss of SIW power divider with and without CSRRs for adjusted number of via metals.

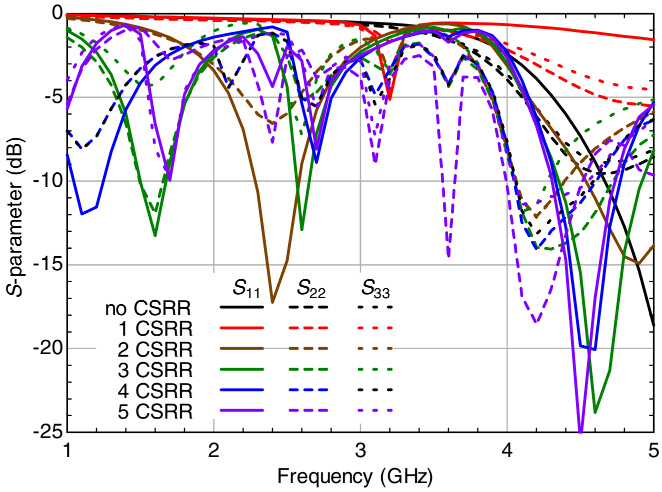

Fig. 5. Return loss of SIW power divider with and without CSRRs for number of via metals of 9.

at the frequency of 0.8GHz. As depicted in Fig. 6, the value of insertion loss for the SIW power divider with the number of via metals of 9 is less than 5dB.

In addition, the number of via metals also contributes to the characteristic of SIW power divider in which this is inline with the increase of number of incorporated CSRRs. It shows that the increase of number of incorporated CSRRs affects to the decrease of frequency response. The more CSRRs is incorporated, the frequency response of SIW power divider will be lower. Moreover, the values of return loss and the insertion loss tend to be poorer for the higher number of CSRRs incorporation although the poorness of quality shows no particular pattern. It is also found that return loss and insertion loss are influenced by the distance between CSRRs. While the width of the passband region for each SIW power divider has strong correlation with the values of return loss and insertion loss on each port.

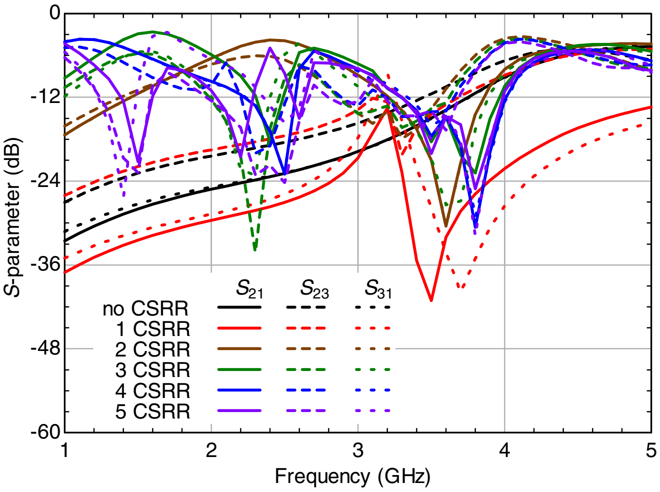

Fig. 6. Insertion loss of SIW power divider with and without CSRRs for varied number of via metals of 9.

IV. CONCLUSION

The design of SIW power divider and its performance analysis affected by the number of incorporated CSRRs have been presented. The SIW power divider deployed on a 1.6mm thick FR4 epoxy dielectric substrate has been designed to have adjusted length of SIW surface according to the number of incorporated CSRR as well as via metals. From the analysis results, in general it was found that the number of incorporated CSRRs have affected remarkably the frequency response, return loss, and insertion loss of SIW power divider. Meanwhile, when the number of via metals were to be fixed of 9 pieces, there was a shift in frequency response to the low frequency region along with the increase of number of incorporated CSRRs.

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